

What is claimed is:

1. A frequency multiplier comprising:
 - a delay circuit that receives a first clock signal having a first frequency and outputs a delayed clock signal, the delay circuit producing the delayed clock signal by applying a time delay to the first clock signal;
 - an XOR gate that receives the first clock signal and the delayed clock signal, performs an XOR operation on the first clock signal and the delayed clock signal, and outputs the second clock signal; and
 - a control circuit that detects a phase difference between the first clock signal and the delayed clock signal, and outputs a control signal to the delay circuit corresponding to the detected phase difference,
wherein the control signal controls a duration of the time delay applied to the first clock signal by the delay circuit.
2. A frequency multiplier according to claim 1, wherein:
the control signal includes a plurality of bit signals corresponding to the detected phase difference, each bit signal having a logic state.
3. A frequency multiplier according to claim 1, wherein:
the control circuit includes
a phase detector that receives the first clock signal and the delayed clock signal and

outputs a first voltage and a second voltage, the first and second voltages corresponding to the detected phase difference between the first clock signal and the delayed clock signal;

a comparator that compares the first voltage and the second voltage, generates a comparison result and outputs a logic signal having a predetermined logic state corresponding to the comparison result; and

a counter that outputs the control signal in synchronization with the first clock signal, wherein the logic state of the plurality of bit signals correspond to the logic signal output from the comparator.

4. A frequency multiplier according to claim 3, wherein:

the phase detector includes

a first voltage control unit that receives the first clock signal and the delayed clock signal and controls the first voltage in response to logic states of the first clock signal and the delayed clock signal, and

a reset signal generating unit that generates a reset signal using the first clock signal and the delayed clock signal;

a reset unit that sets the first voltage and the second voltage at a reset voltage level in response to the reset signal; and

a second voltage control unit that receives the reset signal and controls the second voltage in response to the reset signal.

5. A frequency multiplier according to claim 4, wherein:

the first voltage control unit increases the first voltage when the first clock signal has a first logic state and the delayed clock signal has a second logic state;

the first voltage control unit decreases the first voltage when the first clock signal and the delayed clock signal have the first logic state; and

when the first clock signal has the second logic state, the first voltage control unit and the second voltage control unit set the first voltage and the second voltage to a reset voltage.

6. A frequency multiplier according to claim 1, wherein:

the control signal includes a plurality of bit signals, each bit signal having a logic state,

wherein the duration of the time delay applied to the first clock signal by the delay circuit corresponds to the logic states of the bit signals.

7. A frequency multiplier according to claim 6, wherein:

the delay circuit includes a plurality of inversion circuit groups, the inversion circuit groups being serially connected between input and output terminals of the delay circuit, and further wherein

each inversion circuit group includes a plurality of inversion circuits connected in parallel, an incremental time delay applied by each inversion circuit group is controlled in response to activation of the inversion circuits, in which at least one inversion circuit is activated in response to the control signal, the incremental time delays applied by each inversion group determining the time delay applied by the delay circuit.

8. The frequency multiplier of claim 1, wherein:
the second clock signal has a second frequency that is twice that of the first frequency.

9. A frequency multiplier comprising:
a delay circuit that receives a first clock signal, applies a time delay to the first clock signal and outputs a delayed clock signal;
a logic circuit that receives the first clock signal and the delayed clock signal, synthesizes the first clock signal and the delayed clock signal and outputs a second clock signal;
a phase detector that detects a phase difference between the first clock signal and the delayed clock signal and outputs a first voltage, wherein the first voltage corresponds to the detected phase difference, and a second voltage, wherein the second voltage is a reference voltage;
a comparator that compares the first voltage and the second voltage to generate a comparison result and outputs a logic signal corresponding to the comparison result; and
a counter that outputs a digital signal to the delay circuit, the digital signal including N-bits having logic states corresponding to the logic signal,
wherein the digital signal is synchronized with the first clock signal, and
further wherein the time delay applied by the delay circuit corresponds to the digital signal.

10. A frequency multiplier according to claim 9, wherein:

the first voltage increases during a first period of the first clock signal;
the first voltage decreases during a second period of the first clock signal; and
the level of the first voltage is set to be approximately equal to the second voltage
during a third period of the first clock signal.

11. A frequency multiplier according to claim 10, wherein:

the first period starts at a rising edge of the first clock signal and ends at a rising edge
of the delayed clock signal;
the second period starts at the rising edge of the delayed clock signal and ends at a
falling edge of the first clock signal; and
the third period starts at the falling edge of the first clock signal and ends at a falling
edge of the delayed clock signal.

12. A frequency multiplier according to claim 9, wherein:

a value of the digital signal of N-bits output from the counter is adjusted in response to
the logic signal by changing the logic state of at least one of the N-bits of the digital signal.

13. A frequency multiplier according to claim 9, wherein:

the first clock signal has a first frequency; and
the second clock signal has a second frequency, wherein the second frequency is twice
that of the first frequency.

14. A method of frequency multiplication comprising:

- (a) receiving a first clock signal and applying a time delay to the first clock signal to generate a delayed clock signal;
- (b) performing an XOR operation on the first clock signal and the delayed clock signal to generate a second clock signal;
- (c) detecting a phase difference between the first clock signal and the delayed clock signal and generating a digital control signal corresponding to the detected phase difference; and
- (d) using the digital control signal to set a duration of the time delay applied to the first clock signal.

15. A method of frequency multiplication according to claim 14, wherein:

receiving the first clock signal and applying a time delay to the first clock signal to generate a second clock signal includes

receiving the digital control signal; and

setting a duration of the time delay according to a logic state of the digital control signal.

16. A method of frequency multiplication according to claim 14, wherein:

detecting a phase difference between the first clock signal and the delayed clock signal and generating a digital control signal corresponding to the detected phase difference includes

- (c1) receiving the first clock signal and the delayed clock signal;

(c2) generating a first voltage and a second voltage corresponding to the detected phase difference;

(c3) comparing the first voltage and the second voltage to generate a voltage comparison result;

(c4) generating a logic signal having a predetermined logic state corresponding to the voltage comparison result;

(c5) setting the logic state of the digital control signal to correspond to the logic signal; and

(c6) outputting the digital control signal in synchronization with the first clock signal.

17. A method of frequency multiplication according to claim 16, wherein:
setting the logic state of the digital control signal to correspond to the logic signal includes

(c51) incrementing or decrementing a value of the digital control signal in response to the logic signal.

18. A method of frequency multiplication according to claim 16, wherein:
generating a first voltage and a second voltage corresponding to the detected phase difference includes

increasing the first voltage when the first clock signal has a first logic state and the delayed clock signal has a second logic state; and

decreasing the first voltage when the first clock signal has the first logic state and the delayed clock signal has the first logic state.

19. A method of frequency multiplication according to claim 18, wherein: generating a first voltage and a second voltage corresponding to the detected phase difference includes

setting the first voltage and the second voltage to a reset voltage value when the first clock signal has the second logic state.

20. A method of frequency multiplication according to claim 14, wherein:

(a) receiving a first clock signal and applying a time delay to the first clock signal to generate a delayed clock signal includes inputting a first clock signal into a delay circuit and outputting a delayed clock signal from the delay circuit;

(b) performing an XOR operation on the first clock signal and the delayed clock signal to generate a second clock signal includes inputting the first clock signal and the delayed clock signal into a XOR circuit and outputting a second clock signal from the XOR circuit;

(c) detecting a phase difference between the first clock signal and the delayed clock signal and generating a digital control signal corresponding to the detected phase difference includes

inputting the first clock signal and the delayed clock signal into a phase detector and outputting a first voltage and a second voltage from the phase detector,

sensing the first voltage and the second voltage in a comparator and outputting a logic signal from the comparator,

inputting the first clock signal and the logic signal into a counter and outputting a digital control signal; and

(d) using the digital control signal to set a duration of the time delay applied to the first clock signal includes using the logic state of N-bits included in the digital control signal to activate at least one of a plurality of inversion circuits, wherein the duration of the time delay applied to the first clock signal corresponds to the activated inversion circuits.